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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,481	10/02/2003	Shiao-Shien Chen	NAUP0549USA	2480

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,481	CHEN ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: element 37 (see, for example, page 15, line 3). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because Fig. 2 and Fig. 4 disagree with each other. Fig. 2 discloses a tunneling connection between an extended N+ gate section 36 over a **P-type electrically isolated body 15** in a P-type silicon thin film 16. However, Fig. 4 discloses the same tunneling connection wherein the extended N+ gate section 36 is now over a **N-type extended body region 52**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the

appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: there are numerous spacing errors (for example, "apartially" in paragraph [0015]) between words throughout the specification.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 7 thru 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In lines 14 and 15 of claim 7, it is unclear what the applicant is referring to in the limitation "first end" and "second end" and whether it is referring to the polysilicon gate or another structure in the SOI MOS device. For the sake of compact prosecution, the Examiner is interpreting the "first end" and "second end" to refer to the polysilicon gate, however, proper clarification and/or correction are required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claim 1, 3, 4, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ebina 6,521,948 B2. Ebina discloses (see, for example, FIG. 2 and FIG. 1) a partially depleted SOI transistor comprising a p- region (well of first conductivity type) 14, silicon single crystal layer (thin film body), silicon substrate (support substrate) 10, buried oxide film (buried oxide layer) 12, gate insulating film (gate dielectric layer) 22, p+ conductive portion (first gate section of first conductivity type) 56, n+ gate electrode (second gate section of second conductivity type) 24, p+ region (extended well region) 16, source region 40, and drain region 38. A tunneling connection is formed between the p+ conductive portion 56 and p+ region 16. In column 8, lines 66 - column 9, line 1, Ebina discloses the gate electrode and p+ conductive potion being made of

polysilicon. Also, in column 12, lines 59-63, Ebina discloses the transistors may be partially depleted.

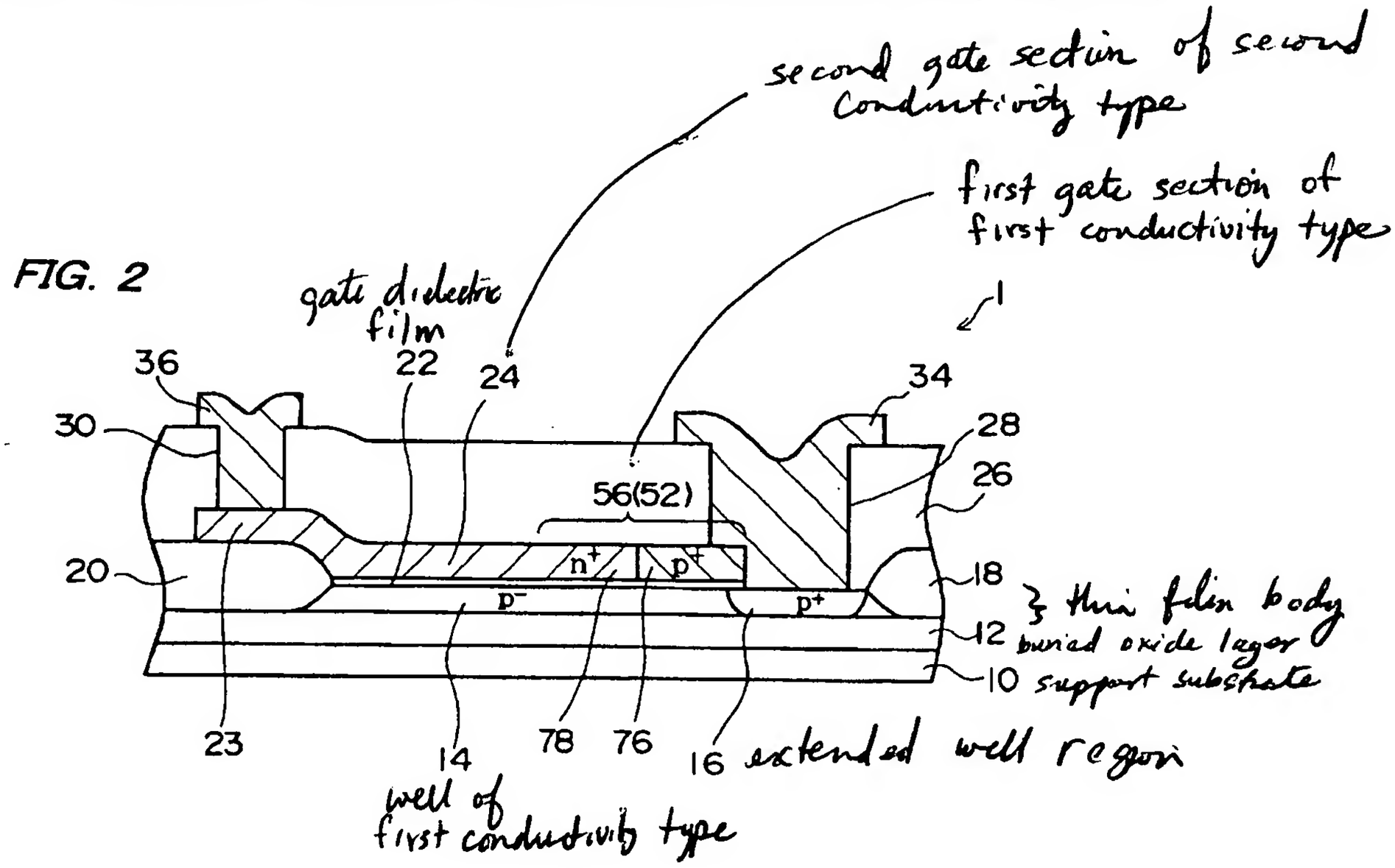

FIG. 2

Regarding claim 3, see, for example, column 8, lines 58-62, wherein Ebina discloses the gate insulating film having a thickness of 4 nm to 10 nm (40-100 angstroms).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina '948 B2 as applied to claims 1, 3, 4, and 6 above, and further in view of Mistry et al. 5,821,575. Ebina does not disclose said gate dielectric layer being selected from the group consisting of silicon dioxide,

nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer. However, Mistry discloses (see, for example, column 5, lines 52-59) a semiconductor device comprising an electrical insulating layer (gate dielectric layer) 44 and a gate electrode 48. Mistry further discloses the electrical insulating layer being silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of invention to have said gate dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer in order to have adequate insulation between the gate electrode and the silicon single crystal layer, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina '948 B2 as applied to claims 1, 3, 4, and 6 above, and further in view of Ohyanagi et al. 6,657,257 B2. Ebina does not disclose said first conductivity type being N type, and said second conductivity type being P type. However, Ohyanagi discloses (see, for example, column 3, lines 47-50) a semiconductor device wherein the semiconductor device may go from P-type to N-type by simply reversing the conductivity type of each semiconductor layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said first conductivity type being N type, and said second conductivity type being P type in order to form a semiconductor device of reverse conductivity type.

11. Claims 7, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina 6,521,948 B2 in view of Ebina 6,734,500 B2. Ebina discloses (see, for example, FIG. 2 and FIG. 1) a partially depleted SOI transistor comprising a single crystal layer (silicon wafer having a thin film body), silicon substrate (supporting substrate) 10, buried oxide film (buried oxide layer) 12, p- region (well) 14, gate insulating film (gate dielectric layer) 22, n+ gate electrode (polysilicon gate of first conductivity type) 24, field oxide film (first oxide filled trench) 20, field oxide film (second oxide filled trench) 18, p+ type portion (portion of one of said ends of said polysilicon gate is implanted with ions of second conductivity type opposite to said first conductivity type) 76, source region 40, and drain region 38. A tunneling connection is formed between the p- region 14 and p+ type portion 76. Ebina '948 does not disclose a second end over a second oxide filled trench. However, Ebina '500 discloses (see, for example, Fig. 2 and Fig. 4) a semiconductor device comprising a gate electrode layer 110 wherein the gate electrode comprises a first and second end over an element isolation region 14. In column 10, lines 8-20, Ebina discloses the gate electrode layer extending from the element isolation region 14 to the other element isolation region 14. It would have been obvious to one of ordinary skill in the art at the time of invention to have a second end over a second oxide filled trench in order to increase the coverage over the single crystal layer (in between the oxide filled trenches).

Regarding claim 9, see, for example, column 8, lines 58-62, wherein Ebina '948 discloses the gate insulating film having a thickness of 4 nm to 10 nm (40-100 angstroms).

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina '948 B2 in view of Ebina '500 B2 as applied to claims 7, 9, 10, and 12 above, and further in view of Mistry

et al. 5,821,575. Ebina '948 B2 in view of Ebina '500 B2 does not disclose said gate dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer. However, Mistry discloses (see, for example, column 5, lines 52-59) a semiconductor device comprising an electrical insulating layer (gate dielectric layer) 44 and a gate electrode 48. Mistry further discloses the electrical insulating layer being silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of invention to have said gate dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer in order to have adequate insulation between the gate electrode and the silicon single crystal layer, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ebina '948 B2 in view of Ebina '500 B2 as applied to claims 7, 9, 10, and 12 above, and further in view of Ohyanagi et al. 6,657,257 B2. Ebina '948 B2 in view of Ebina '500 B2 does not disclose said first conductivity type being P type, and said second conductivity type being N type. However, Ohyanagi discloses (see, for example, column 3, lines 47-50) a semiconductor device wherein the semiconductor device may go from P-type to N-type by simply reversing the conductivity type of each semiconductor layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said first conductivity type being P type, and said

second conductivity type being N type in order to form a semiconductor device of reverse conductivity type.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
August 28, 2004